EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	("6324515".pn. or "6977877".pn.) frame	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 12:18
L2	1	"6594444".PN.	USPAT; USOCR	AND	ON	2006/02/28 08:32
L3	1	"6577589".PN.	USPAT; USOCR	AND	ON	2006/02/28 08:33
L4	1	"6430533".PN.	USPAT; USOCR	AND	ON	2006/02/28 08:33
L5	1	"6360204".PN.	USPAT; USOCR	AND	ON	2006/02/28 08:34
L6	1	"6272153".PN.	USPAT; USOCR	AND	ON	2006/02/28 08:35
L7	1	"6108633".PN.	USPAT; USOCR	AND	ON	2006/02/28 08:35
L8	1	"5987417".PN.	USPAT; USOCR	AND	ON	2006/02/28 08:36
L9	1	"5933398".PN.	USPAT; USOCR	AND	ON	2006/02/28 08:37
L10	1	"5748835".PN.	USPAT; USOCR	AND	ON	2006/02/28 08:37
L11	2	("6324515".pn. or "6977877".pn.) format	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 09:48
L12	1	("6324515".pn. or "6977877".pn.) "22"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 08:47
L13	1	("6324515".pn. or "6977877".pn.) integrat$	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 08:48

EAST Search History

L14	0	("6324515".pn. or "6977877".pn.) periodic$	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 08:48
L15	1	("6324515".pn. or "6977877".pn.) detect$	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 08:48
L16	1	("6324515".pn. or "6977877".pn.) table	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 10:38
L17	0	("6324515".pn. or "6977877".pn.) (code ADJ1 word)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 09:53
L18	97	(select$2 or selecting) decod$ format (detect$2 or detecting)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/02/28 10:21
L19	0	(select$2 or selecting) decod$ format (detect$2 or detecting)(code ADJ1 word and header and frame)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/02/28 10:22
L20	0	(select$2 or selecting) decod$ (detect$2 or detecting)(code ADJ1 word and header and frame)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/02/28 10:22
L21	1	(select$2 or selecting) decod$ (code ADJ1 word and header and frame)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/02/28 10:24

EAST Search History

L22	18	decod$ (code ADJ1 word and header and frame ADJ1 synchronization)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/02/28 10:25
L23	0	("6324515".pn. or "6977877".pn.) 22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 10:38
L24	1	("6324515".pn. or "6977877".pn.) "22"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 10:39
L25	1	("6324515".pn. or "6977877".pn.) analysis	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 10:40
L26	1	("6324515".pn. or "6977877".pn.) analyzer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 10:41
L27	2	("6324515".pn. or "6977877".pn.) identifying	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 10:41
L28	482	(704/500,704/201).CCLS.	USPAT	OR	OFF	2006/02/28 12:18
L29	1850	(341/50,51,106,55).CCLS.	USPAT	OR	OFF	2006/02/28 12:30
L30	897	(704/500,201).CCLS.	USPAT	OR	OFF	2006/02/28 12:30
L31	457	(369/47.15-47.19).CCLS.	USPAT	OR	OFF	2006/02/28 12:30
S1	3	"2001024568"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/27 10:09

EAST Search History

S2	0	"2001/024568"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/27 10:10
S3	58	mori NEAR1 taro	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/27 10:20
S4	3	"6330666".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/27 10:22
S5	2	"6324515".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/27 10:24
S6	204	header (switching or switch$2) decoders	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/02/27 10:26
S7	204	header (switching or switch$2) "decoders"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/02/27 10:27
S8	6	header (switching or switch$2) "decoders" format	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/02/27 10:33
S9	15	header (switching or switch$2) decod$ formats	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/02/27 10:51

EAST Search History

S10	20	header (select$2 or selecting) decod$ formats	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/02/27 12:25
S11	4	"6324515".pn. or "6977877".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/27 12:12
S12	1	("6324515".pn. or "6977877".pn.) frame header	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/27 12:27
S13	0	("6324515".pn. or "6977877".pn.) frame header (code ADJ1 word)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 08:23
S14	0	("6324515".pn. or "6977877".pn.) frame header (codeword)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/27 12:17
S15	0	("6324515".pn. or "6977877".pn.) frame header pattern	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/27 12:16
S16	0	("6324515".pn. or "6977877".pn.) pattern	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/27 12:16
S17	0	("6324515".pn. or "6977877".pn.) (codeword)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/28 09:53

EAST Search History

S18	1	("6324515".pn. or "6977877".pn.) logic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/02/27 12:22
S19	4	header (select$2 or selecting) decod$ format (detect$2 or detecting)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/02/27 12:26
S20	179	((369/47.15,369/47.16,369/47.19, 369/47.2) or (,369/47.22,369/47. 23)).CCLS.	USPAT	OR	OFF	2006/02/28 12:29

Terms used **decoder selecting header** Found **310** of **171,143**

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Best 200 shown Relevance scale

1 Robust header compression (ROHC) in next-generation network processors
David E. Taylor, Andreas Herkersdorf, Andreas Döring, Gero Dittmann
August 2005 **IEEE/ACM Transactions on Networking (TON)**, Volume 13 Issue 4
Publisher: IEEE Press
Full text available: pdf(849.58 KB) Additional Information: full citation, abstract, references, index terms

Robust Header Compression (ROHC) provides for more efficient use of radio links for wireless communication in a packet switched network. Due to its potential advantages in the wireless access area and the proliferation of network processors in access infrastructure, there exists a need to understand the resource requirements and architectural implications of implementing ROHC in this environment. We present an analysis of the primary functional blocks of ROHC and extract the architectural implic ...

Keywords: ASIC, ASIP, FPGA, ROHC, hardware assist, header compression, network processor, reconfigurable hardware

2 VLSI design: Quality-of-service and error control techniques for network-on-chip architectures
Praveen Vellanki, Nilanjan Banerjee, Karam S. Chatha
April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press
Full text available: pdf(474.65 KB) Additional Information: full citation, abstract, references, index terms

Networks-on-a-Chip (NoC) has been proposed as a solution for addressing the design challenges of future high-performance nanoscale architectures. Real-time applications require multiple service levels to account for traffic with low delay jitter. As technology scales toward deep submicron, on-chip interconnects are becoming more and more sensitive to noise sources such as power supply noise, crosstalk, radiation induced effects, that are likely to reduce the reliability of data. This paper addre ...

Keywords: correction, error detection, interconnection, networks, networks-on-chip, performance, power, quality-of-service

3 Ariadne—an adaptive router for fault-tolerant multicomputers
J. D. Allen, P. T. Gaughan, D. E. Schimmel, S. Yalamanchili
April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST**

annual international symposium on Computer architecture ISCA '94, Volume 22 Issue 2
Publisher: IEEE Computer Society Press, ACM Press
Full text available: pdf(1.21 MB) Additional Information: full citation, abstract, references, citings, index terms

Adaptive routing has been proposed as a means of improving performance and fault-tolerance in multicomputer networks. While a number of algorithms have been proposed, few adaptive routers have been implemented in hardware. This paper presents the design and implementation of Ariadne --- a prototype single chip, hardware router. The primary motivation is tolerance to link and router failures, while reconciling conflicting demands on performance. This is achieved by implementing the *m*-misro ...

4 An architecture for extended abstract data flow
Vason P. Srini
May 1981 **Proceedings of the 8th annual symposium on Computer Architecture**
Publisher: IEEE Computer Society Press
Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references, citings, index terms

A distributed computer system environment for executing extended abstract data flow graphs (EDFGs) is presented. Sequencing functions in EDFGs depends on the availability of data. Since the functions are free of side effects, unrelated functions can be executed in parallel if the required data is available. The environment comprises an organization of conventional or data flow processors and the kernel functions of a distributed operating system. The processors are organized in g ...

5 Steganography I: Perturbed quantization steganography with wet paper codes
Jessica Fridrich, Miroslav Goljan, David Soukal
September 2004 **Proceedings of the 2004 workshop on Multimedia and security MM&Sec '04**
Publisher: ACM Press
Full text available: pdf(396.88 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we introduce a new approach to passive-warden steganography in which the sender embeds the secret message into a certain subset of the cover object without having to share the selection channel with the recipient. An appropriate information-theoretical model for this communication is writing in memory with (a large number of) defective cells [1]. We describe a simple variable-rate random linear code for this channel (the "wet paper" code) and use it to develop a new steganographic ...

Keywords: adaptive, multimedia, quantizer, security, steganalysis, steganography

6 Wormhole routing techniques for directly connected multicomputer systems
Prasant Mohapatra
September 1998 **ACM Computing Surveys (CSUR)**, Volume 30 Issue 3
Publisher: ACM Press
Full text available: pdf(340.68 KB) Additional Information: full citation, abstract, references, citings, index terms

Wormhole routing has emerged as the most widely used switching technique in massively parallel computers. We present a detailed survey of various techniques for enhancing the performance and reliability of wormhole-routing schemes in directly connected networks. We start with an overview of the direct network topologies and a comparison of various switching techniques. Next, the characteristics of the wormhole routing mechanism are described in detail along with the theory behind deadlock-f ...

7 YAPI: application modeling for signal processing systems

E. A. de Kock, W. J. M. Smits, P. van der Wolf, J.-Y. Brunel, W. M. Kruijtzer, P. Lieverse, K. A. Vissers, G. Essink

June 2000 **Proceedings of the 37th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(94.62 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a programming interface called YAPI to model signal processing applications as process networks. The purpose of YAPI is to enable the reuse of signal processing applications and the mapping of signal processing applications onto heterogeneous systems that contain hardware and software components. To this end, YAPI separates the concerns of the application programmer, who determines the functionality of the system, and the system designer, who determines the implementation of the ...

Keywords: Khan process networks, application modeling, model of computation, signal processing, systems-level design

8 Verification, analysis of embedded systems: A fault model notation and error-control scheme for switch-to-switch buses in a network-on-chip

Heiko Zimmer, Axel Jantsch

October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

Publisher: ACM Press

Full text available: pdf(159.38 KB) Additional Information: full citation, abstract, references, citings, index terms

The reliability of a Network-on-Chip will be significantly influenced by the reliability of the switch-to-switch connections. Faults on these buses may cause disturbances on multiple adjacent wires, so that errors on these wires can no longer be considered as statistically independent from one another, as it is expected due to deep submicron effects. A new fault model notation for buses is proposed which can represent multiple-wire, multiple-cycle faults. An estimation method based on this notat ...

Keywords: bus encoding, fault tolerance, network-on-chip

9 Error control schemes for networks: an overview

Hang Liu, Hairuo Ma, Magda El Zarki, Sanjay Gupta

October 1997 **Mobile Networks and Applications**, Volume 2 Issue 2

Publisher: Kluwer Academic Publishers

Full text available: pdf(516.05 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we investigate the issue of error control in wireless communication networks. We review the alternative error control schemes available for providing reliable end-to-end communication in wireless environments. Through case studies, the performance and tradeoffs of these schemes are shown. Based on the application environments and QoS requirements, the design issues of error control are discussed to achieve the best solution.

10 Designing digital video systems: modeling and scheduling

H. J. H. N. Kenter, C. Passerone, W. J. M. Smits, Y. Watanabe, A. L. Sangiovanni-Vincentelli

March 1999 **Proceedings of the seventh international workshop on Hardware/software codesign**

Publisher: ACM Press

Full text available: Additional Information:

pdf(485.34 KB) full citation, references, citings, index terms

11 Low-level router design and its impact on supercomputer system performance
V. Puente, J. A. Gregorio, C. Izu, R. Beivide, F. Vallejo
May 1999 **Proceedings of the 13th international conference on Supercomputing**
Publisher: ACM Press
Full text available: pdf(1.54 MB) Additional Information: full citation, references, index terms

12 A secure multicast protocol with copyright protection
Hao-hua Chu, Lintian Qiao, Klara Nahrstedt, Hua Wang, Ritesh Jain
April 2002 **ACM SIGCOMM Computer Communication Review**, Volume 32 Issue 2
Publisher: ACM Press
Full text available: pdf(301.97 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a simple, efficient, and secure multicast protocol with copyright protection in an open and insecure network environment. There is a wide variety of multimedia applications that can benefit from using our secure multicast protocol, e.g., the commercial pay-per-view video multicast, or highly secure military intelligence video conference. Our secure multicast protocol is designed to achieve the following goals. (1) It can run in any open network environment. It does not rely on any sec ...

Keywords: copyright protection, key distribution, multicast security, watermark

13 Focus on AiroPeek
Gilbert Held
August 2002 **International Journal of Network Management**, Volume 12 Issue 5
Publisher: John Wiley & Sons, Inc.
Full text available: pdf(387.86 KB) Additional Information: full citation, index terms

14 An MPEG-2 decoder case study as a driver for a system level design methodology
Pieter van der Wolf, Paul Lieverse, Mudit Goel, David La Hei, Kees Vissers
March 1999 **Proceedings of the seventh international workshop on Hardware/software codesign**
Publisher: ACM Press
Full text available: pdf(444.79 KB) Additional Information: full citation, references, citings, index terms

15 Algorithms and methodologies for new architectures: Designing real-time H.264 decoders with dataflow architectures
Youngsoo Kim, Suleyman Sair
September 2005 **Proceedings of the 3rd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis CODES+ISSS '05**
Publisher: ACM Press
Full text available: pdf(278.83 KB) Additional Information: full citation, abstract, references, index terms

High performance microprocessors are designed with general-purpose applications in mind. When it comes to embedded applications, these architectures typically perform control-intensive tasks in a System-on-Chip (SoC) design. But they are significantly

inefficient for data-intensive tasks such as video encoding/decoding. Although configurable processors fill this gap by complementing the existing functional units with instruction extensions, their performance lags behind the needs of real-time em ...

Keywords: H.264, WaveScalar, dataflow architecture

16 Session P16: isosurfaces: BLIC: bi-level isosurface compression

Gabriel Taubin
October 2002 **Proceedings of the conference on Visualization '02**
Publisher: IEEE Computer Society

Full text available: pdf(561.66 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we introduce a new and simple algorithm to compress isosurface data. This is the data extracted by isosurface algorithms from scalar functions defined on volume grids, and used to generate polygon meshes or alternative representations. In this algorithm the mesh connectivity and a substantial proportion of the geometric information are encoded to a fraction of a bit per Marching Cubes vertex with a context based arithmetic coder closely related to the JBIG binary image compression ...

Keywords: 3D geometry compression, algorithms, graphics

17 A high-performance object-oriented memory

Craig Hyatt
September 1993 **ACM SIGARCH Computer Architecture News**, Volume 21 Issue 4
Publisher: ACM Press
Full text available: pdf(919.75 KB) Additional Information: full citation, abstract, index terms

The proposed design places a high-performance object memory in a portable peripheral that relieves the host CPU of the burden of object address translation and the constant management of live objects. This flexible approach is designed for the newest generation of high-performance workstations running 32-bit Smalltalk, Lisp, C++ and other COP (object oriented programming) environments. With a two-layer cache and 50ns DRAM object memory, the hardware is capable of accessing object data (including ...

Keywords: RISC, binary-buddy allocation, capability-based protection

18 Wisconsin Architectural Research Tool Set

Mark D. Hill, James R. Larus, Alvin R. Lebeck, Madhusudhan Talluri, David A. Wood
September 1993 **ACM SIGARCH Computer Architecture News**, Volume 21 Issue 4
Publisher: ACM Press
Full text available: pdf(1.16 MB) Additional Information: full citation, citings, index terms

19 Loss profiles: a quality of service measure in mobile computing

Krishanu Seal, Suresh Singh
March 1996 **Wireless Networks**, Volume 2 Issue 1
Publisher: Kluwer Academic Publishers

Full text available: pdf(1.54 MB) Additional Information: full citation, abstract, references, citings, index terms

With rapid technological advances being made in the area of wireless communications it is

expected that, in the near future, mobile users will be able to access a wide variety of services that will be made available over future high-speed networks. The quality of these services in the high-speed network domain can be specified in terms of several QOS parameters. In this paper we identify a new QOS parameter for the mobile environment, called loss profiles, that ensures graceful degradation ...

20 A platform for multimedia information exchange

Chung-Ming Huang, Chung-Ming Lo
April 1994 **Proceedings of the 1994 ACM symposium on Applied computing**
Publisher: ACM Press
Full text available: pdf(496.28 KB) Additional Information: full citation, references, index terms

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Results for "((decoder <in>metadata) <and> (selecting <in>metadata))<and> (header&..." e-mail
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((decoder <in>metadata) <and> (selecting <in>metadata))<and> (header<in>me Search

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IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **Decoder-assisted frame synchronization for packet transmission**
Howlader, M.M.K.; Woerner, B.D.;
Selected Areas in Communications, IEEE Journal on
Volume 19, Issue 12, Dec. 2001 Page(s):2331 - 2345
Digital Object Identifier 10.1109/49.974600
AbstractPlus | References | Full Text: PDF(273 KB) IEEE JNL
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